MEMTECH

BPK 74
4-MEGABIT BUBBLE MEMORY SUBSYSTEM

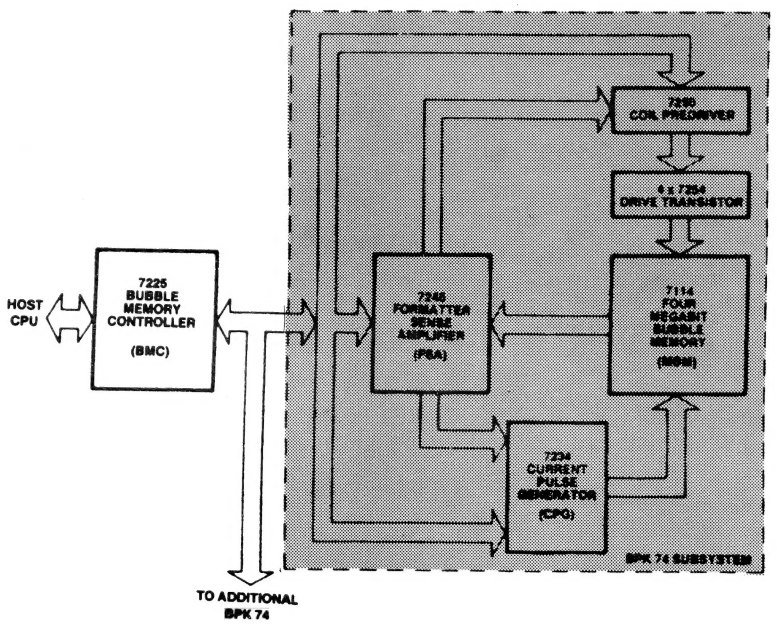
BPK 74-4	10°C (Ambient) to 55°C (Case)
BPK 74-1	0°C (Ambient) to 75°C (Case)

- **4-Megabit (512K Byte) Non-Volatile, Solid-State, Read/Write Bubble Memory Subsystem**
- **Interfaces to Host Microprocessor Via Additional Bubble Memory Controller**
- **Contains Bubble Memory and ICs for Production with 4-Megabit Bubble Memory**
- **Modularity Provides Expansion Up to Eight Subsystems Per Controller**
- **Maximum Data Rate of 200K bit/sec with One Subsystem**
- **Maximum Data Rate of 200K byte/sec with Eight Subsystems in Parallel and Time Multiplexed**
- **Power Fail Circuitry Integrated into 7225 Controller**
- **Average Random Access Time of 88 ms**
- **Contains Internally Packaged Z-Coil**
- **Bubble Memory in 20-Lead Package**

The BPK 74 Bubble Memory Subsystem is a modular building block used to design bubble memory systems. In a complete bubble memory system, a 7225 Bubble Memory Controller (BMC) interfaces the BPK 74 subsystem to the host processor.

The modular MemTech subsystem provides a path for density expansion. One BMC can interface up to eight 4-Megabit subsystems. Thus, a 4-Megabit (512K Byte) system can be expanded up to a 4-Megabyte system by adding subsystems. BMC's can be combined in parallel to further expand the system memory capacity.

Together, the BPK 74 Bubble Storage Subsystem and a 7225 controller provide a reliable mass storage system for any application. This bubble memory system can be customized to the particular layout and form factor of many different systems.


HOST CPU
7225 BUBBLE MEMORY CONTROLLER (BMC)
7240 FORMATTER SENSE AMPLIFIER (FSA)
7114 FOUR MEGABIT BUBBLE MEMORY
7234 CURRENT PULSE GENERATOR (CPG)
BPK 74 SUBSYSTEM
TO ADDITIONAL BPK 74

0001-1

Figure 1. Block Diagram of a 512K Byte Bubble Storage System

© MemTech Technology Corporation, 1987

October 1987
Order Number: 152626-001

SPECIFICATIONS

Capacity

512K Byte per BPK 74
Maximum of 8 BPK 74 per 7225 Controller

Performance

Avg. Access Time . . . . . 88 ms

Data Organization (Single Subsystem)

64 bytes per page
8192 pages per BPK 74

Addressing Scheme

Logical page number

Environmental

Temperature: See BPK 74 Temperature Range
Operating Humidity: 0–95% Non-Condensing

DATA TRANSFER RATES (Examples of System Configurations)

Parameter	One BPK 74 Unit	Eight BPK 74 Operated in Parallel
Capacity	512 kilobytes	4096 kilobytes
Average Data Rate (kilobits/sec)	136	1088
Maximum Data Rate (kilobits/sec) (Burst)	200	1600

BPK 74 POWER SUPPLY REQUIREMENTS

Voltage	Margin	Power Off/Power Fail Decay Rate
+12 Volt	±5%	less than 1.10 volts/ms for 70 μs min.
+5 Volt	±5%	less than 0.45 volts/ms for 70 μs min.

- Power on voltage rate of rise— no restrictions

BPK 74 POWER CONSUMPTION

Breakdown By Device	+5 (Watts)		+12 (Watts)				Total (Watts)			
	Active & Standby		Active		Standby		Active		Standby	
	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.
7225	1.05	0.48	0.00	0.00	0.00	0.00	1.05	0.48	1.05	0.48
7114	0.00	0.00	2.25	1.74	0.38	0.24	2.25	1.74	0.38	0.24
7234	0.24	0.15	0.44	0.24	0.25	0.14	0.68	0.39	0.49	0.29
7245	0.63	0.43	0.38	0.06	0.38	0.06	1.01	0.49	1.01	0.49
7250	0.00	0.00	0.95	0.48	0.06	0.05	0.95	0.48	0.06	0.05
7254 (4)	0.00	0.00	3.14	2.45	0.00	0.00	3.14	2.45	0.00	0.00
BPK-74 Kit	0.87	0.58	*6.02	4.97	*0.86	0.49	6.89	5.55	1.94	1.07
BPK-74 & 7225	1.92	1.06	*6.02	4.97	*0.86	0.49	7.94	6.03	2.99	1.55

NOTES:
*Maximum numbers are based on an average of the absolute maximum and the typical numbers.
$P_{MAX(kit)} = \Sigma Ptyp + \sqrt{\Sigma (Pmax - Ptyp)^2}$
BPK74 kit includes the 7114, 7234, 7245, and four 7254's.
Maximum power based on; $V_{CC} = 5.25V$, $V_{DD} = 12.6V$.
Typical power based on; $V_{CC} = 5V$, $V_{DD} = 12V$.

Functional Description

A BPK 74 subsystem and a 7225 controller comprise a complete bubble memory system. The 4-Megabit BMC, the 7225, provides the interface between the host microprocessor and the bubble memory subsystem and provides all the timing and control signals to the subsystem. The user interface of the BMC is compatible with standard microprocessors and microcontrollers. The BMC is a software driven device utilizing 18 convenient commands. The design engineer's primary responsibility is interfacing to the BMC. This is comparable to interfacing to a disk drive controller.

The BPK 74 consists of one 4-Megabit Magnetic Bubble Memory (MBM) and additional support IC's (see Figure 1). The complete family of LSI support circuits has been designed to handle the complex analog interface associated with bubble devices. The support IC's for the MBM consists of—a 7250 Coil Predriver (CPD), four 7254 VMOS FET Transistor Packs, a 7234 Current Pulse Generator (CPG) and a 7245 Formatter Sense Amplifier (FSA).

Data integrity is insured by the automatic error correction designed into the BPK 74.

The average random access time of a 4-Megabit subsystem is 88 ms with a 200K bit/sec maximum data transfer rate. When operating several subsystems in parallel, the BMC uses time division multiplexing. Therefore, the maximum data rate increases proportional to the number of bubbles operated in parallel.

Operating subsystems serially, one MBM being accessed at a time, the maximum data transfer rate is still 200K bit/sec. If low power consumption is a critical design goal, the bubble memory subsystem can be powered down when it is not being accessed, thus reducing the average power consumption.

The data in the 4-Megabit subsystem is organized in 8192 pages, each with 64 bytes. Conceptually, the data organization with pages is analogous to a disk system's sectors. In systems with multiple bubble memories, the page size can vary from 64 bytes to 512 bytes depending on the number of subsystems and whether or not they are operating in parallel or in serial. (See Table 6 in the 7225 BMC datasheet).

The core components in the subsystem are described in more detail in the remainder of this data sheet.

BPK 74 FUNCTIONAL DESCRIPTION

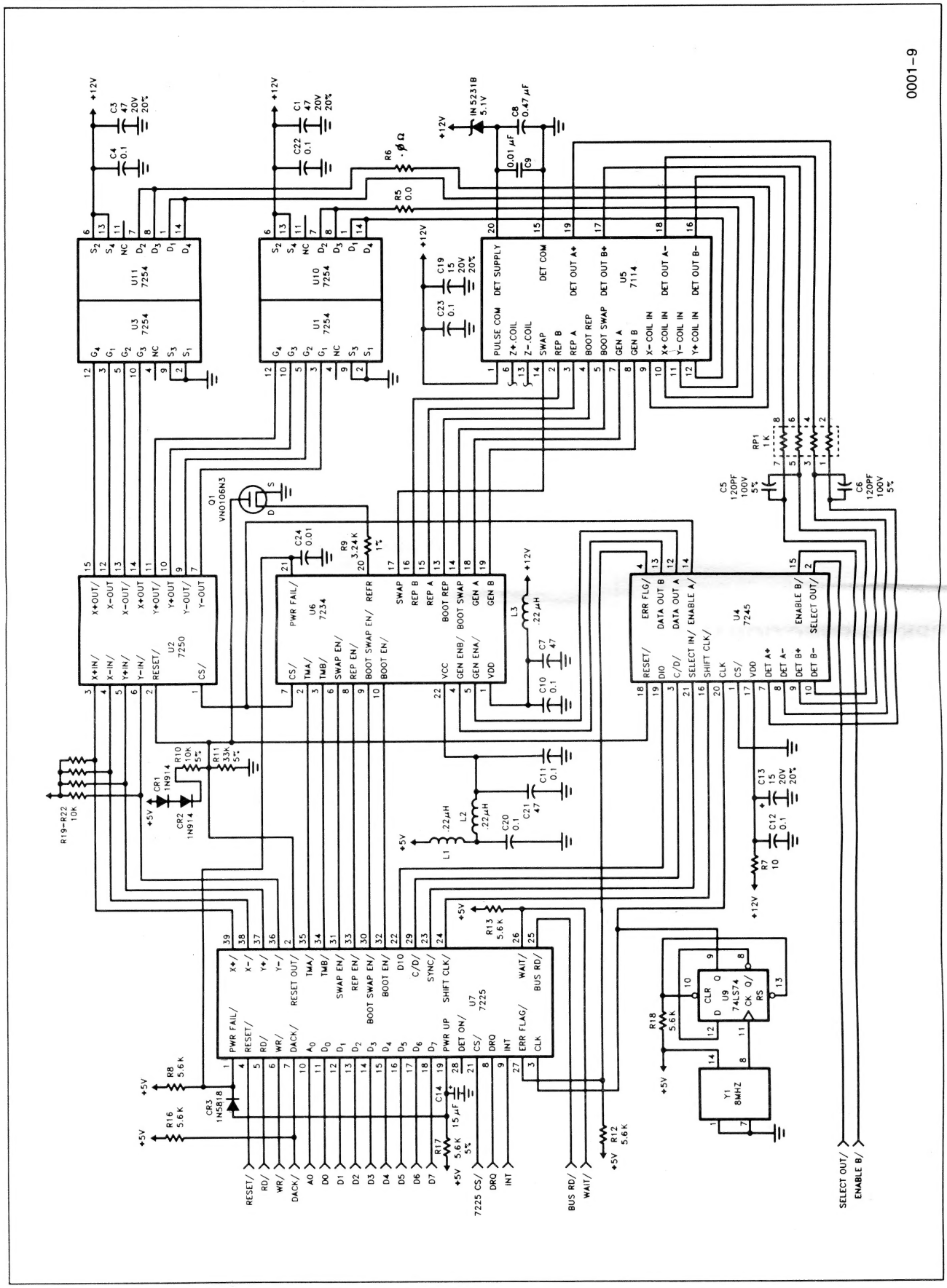
Item	Description	Part Number
4-Megabit Bubble Memory (MBM)	20-pin leaded package that provides 4 megabits of non-volatile storage.	7114
Current Pulse Generator (CPG)	Converts digital timing signals to analog current pulses suited to the drive requirements of the MBM. The CPG provides the replicate, swap, generate, boot replicate, and bootswap pulses required by the MBM. 22 Pin DIP package.	7234
Dual Formatter/Sense Amp (FSA)	Provides direct interface to the Bubble Memory. The FSA contains on-chip sense amplifiers, a full FIFO data block buffer, burst error detection and correction circuits, and circuitry for handling of the bubble memory redundant loops. 22 Pin DIP package.	7245
Coil Predriver	Provides the high voltage, high current outputs to drive the coil drive transistors. 16 Pin DIP package.	7250
MOSFET Coil Drive Transistors (4)	Switches the required current to drive the X and Y coils of the Bubble Memory. 14 Pin DIP package.	7254

For additional packaging information see the packaging information section.

BPK 74 TEMPERATURE RANGE

Bubble Memory Case Temperature Range		Support Circuits Ambient Operating Temperature Range	Description
Operating	Non-Volatile Storage		
+10°C to +55°C	−20°C to +70°C	0° to 70°C	4-Megabit Bubble Subsystem Storage
0°C to +75°C	−40°C to +95°C		

4-MEGABIT SYSTEM SCHEMATIC



SYSTEM COMPONENTS

7114 PIN DESCRIPTION

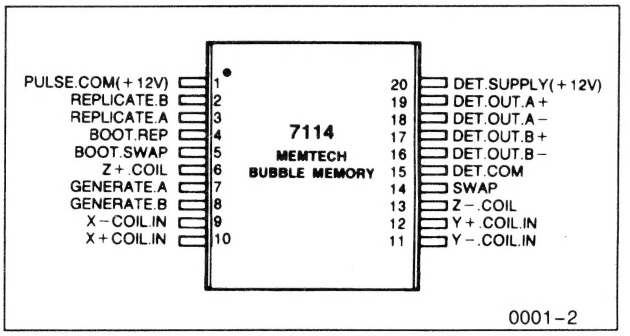


Figure 2. 7114 Pin Configuration

Table 1. 7114 Pin Description

Symbol	Pin No.	I/O	Source/Destination	Description
PULSE.COM	1	I		+12 volt supply pin.
REP.A and REP.B	3, 2	I	7234 CPG	Two-level current pulses for replicating data from storage loops to output track.
BOOT.REP	4	I	7234 CPG	Two-level current pulse input for reading the boot loop.
BOOT.SWAP	5	I	7234 CPG	Single-level current pulse for writing data into the boot loop. This pin is normally used only in the manufacture of the MBM.
GEN.A and GEN.B	7, 8	I	7234 CPG	Two-level current pulses for writing data onto the input track.
X−.COIL.IN X+.COIL.IN	9, 10	I	7254	Terminals for the X or inner coil.
Y−.COIL.IN Y+.COIL.IN	11, 12	I	7254	Terminals for the Y or outer coil.
SWAP	14	I	7234 CPG	Single-level current pulse for swapping data from input track to storage loops.
DET.COM	15	I		Ground return for the detector bridge.
DET.OUT	16–19	O	7245 FSA	Differential pair (A+, A− and B+, B−) outputs which have signals of 10–30 millivolts peak amplitude.
DET.SUPPLY	20	I		+12 volt supply pin.
Z+.COIL Z−.COIL	6, 13	I		Terminals for the Z-Coil.

ABSOLUTE MAXIMUM RATINGS*

7114-4

Relative Humidity (Non-Condensing) 95%
Shelf Storage Temperature (Data Integrity Not Guaranteed) ..... −65°C to +150°C
Voltage Applied to DET.SUPPLY ..... 14 Volts
Voltage Applied to PULSE.COM ..... 14 Volts
Continuous Current between DET.COM and Detector Outputs ..... 20 mA
Coil Current ..... 0.5A D.C.
External Magnetic Field for Non-Volatile Storage ..... 20 Oersteds
Non-Operating Handling Shock 500G
Operating Vibration (20 Hz to 2 kHz) 20G

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

PACKAGING INFORMATION

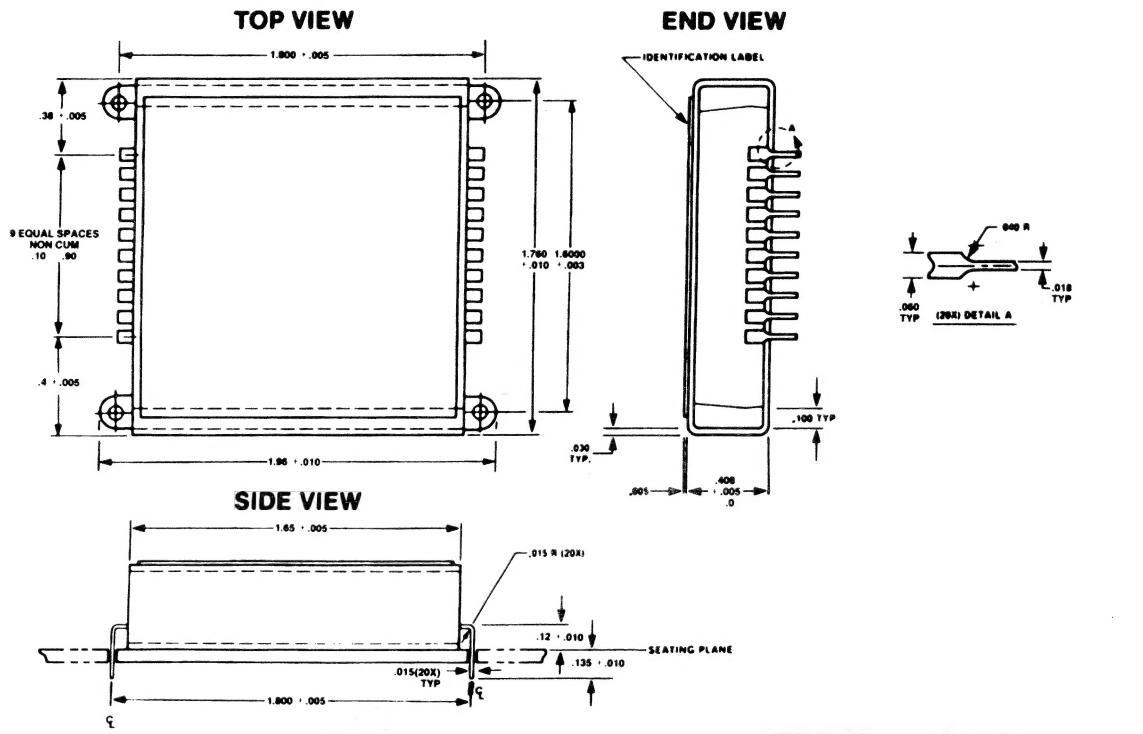


Figure 3. 4-Megabit Leaded Bubble Memory Package

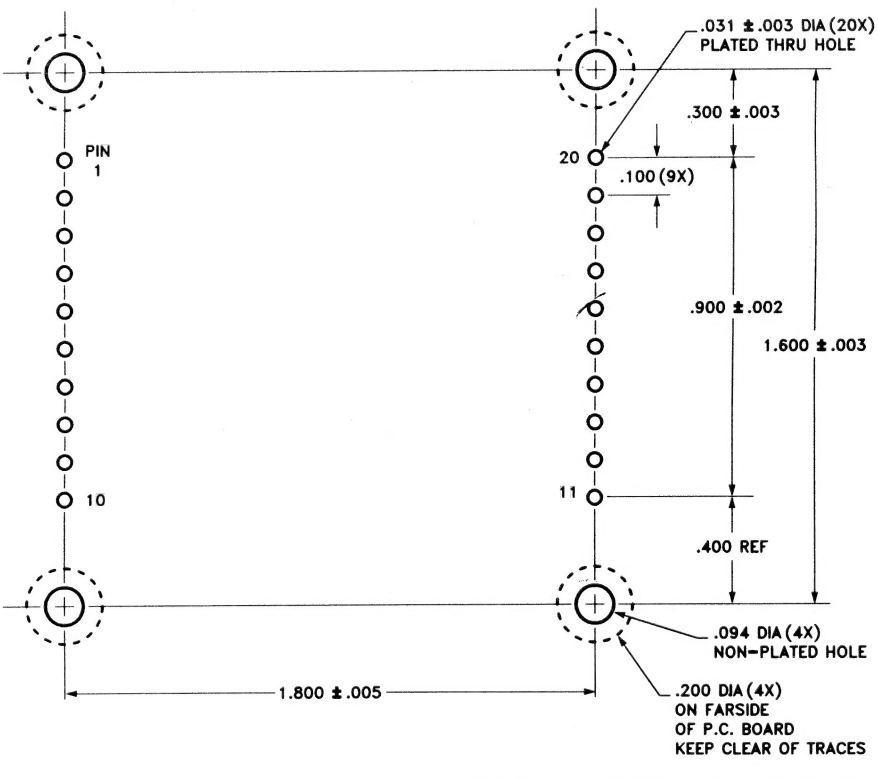


Figure 4. P.C. Board Space Requirements (7114)

7234 PIN DESCRIPTION

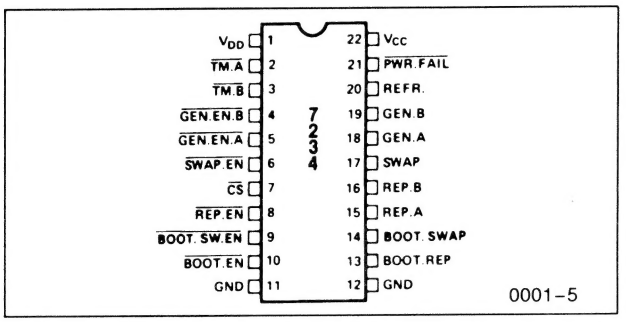


Figure 5. 7234 Pin Configuration

Table 2. 7234 Pin Description

Symbol	Pin No.	I/O	Source/Destination	Description
$\overline{TM.A}$	2	I	7225 BMC	An active low timing signal determining the cut pulse widths of the BOOT.REP, GEN.A, GEN.B, REP.A and REP.B outputs.
$\overline{TM.B}$	3	I	7225 BMC	An active low timing signal determining the transfer pulse widths of the BOOT.REP, GEN.A, GEN.B, REP.A and REP.B outputs.
$\overline{GEN.EN.B}$	4	I	7245 FSA	An active low input enabling the GEN.B output current pulse.
$\overline{GEN.EN.A}$	5	I	7245 FSA	An active low input enabling the GEN.A output current pulse.
$\overline{SWAP.EN}$	6	I	7225 BMC	An active low input enabling the SWAP output.
$\overline{CS}$	7	I	7245 FSA	An active low input for selecting the chip.
$\overline{REP.EN}$	8	I	7225 BMC	An active low input enabling the REP.A and REP.B outputs.
$\overline{BOOT.SW.EN}$	9	I	7225 BMC	An active low input enabling the BOOT.SWAP output current pulse.
$\overline{BOOT.EN}$	10	I	7225 BMC	An active low input enabling the BOOT.REP output current pulse.
BOOT.REP	13	O	7114 MBM	An output providing the current pulse for bootstrap loop replication in the bubble memory.
BOOT.SWAP	14	O	7114 MBM	An output providing a current pulse used for writing data into the bootstrap loop.
REP.A	15	O	7114 MBM	An output providing the current pulse for replication of data in the "A" octants of the bubble memory.
REP.B	16	O	7114 MBM	An output providing the current pulse for replication of data in the "B" octants of the bubble memory.
SWAP	17	O	7114 MBM	An output providing the current pulse for exchanging the data between the input track and the storage loops in the bubble memory.
GEN.A	18	O	7114 MBM	An output providing the current pulse for writing data into the "A" octants of the bubble memory.
GEN.B	19	O	7114 MBM	An output providing the current pulse for writing data into the "B" octants of the bubble memory.
REFR.	20	I	External Resistor	The pin for the reference current generator to which an external resistance must be connected.
$\overline{PWR.FAIL}$	21	O	7225 BMC	An active low, open collector output indicating that either V_{CC} or V_{DD} is below its threshold value.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65 to +150°C
Voltage Input ..... −0.5 to +7V
V_{CC} ..... −0.5 to +7V
V_{DD} ..... −0.5 to +12.6V
Power Dissipation @ 25°C 1W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

D7234 T_A = 0°C to +70°C; V_{CC} = 5.0V +5%, V_{DD} = 12.0V ±5%
D7234-6 T_A = −40°C to +85°C; V_{CC} = 5.0V +5%, V_{DD} = 12.0V ±5%

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
I_{IL}	Input Low Current			−0.4	mA	V_{IL} = 0.4V, V_{CC} = 5.25V
I_H	Input High Current			20	μA	V_{IH} = V_{CC} = 5.25V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_C	Input Clamp Voltage			−1.5	V	I = −18 mA, V_{CC} = 4.75V
I_{CEX1}	Output Leakage Current (All Outputs except PWR.FAIL)			1.0	mA	V_{CC} = 5.25V, V_{DD} = 12.6V
I_{CEX2}	$\overline{\text{PWR.FAIL}}$ Output Leakage Current			40	μA	V_{OH} = V_{CC} = 5.25V
V_{OL}	$\overline{\text{PWR.FAIL}}$ Output Low Voltage			0.4	V	I_{OL} = 4 mA, V_{CC} = 4.75V
I_{CC1}	Current from V_{CC}—Selected		30	45	mA	CS = V_{IL}. V_{CC} = 5.25V
I_{DD1}	Current from V_{DD}—Selected		20	35	mA	CS = V_{IL}, V_{CC} = 5.25V
I_{DD2}	Current from V_{DD}—Power Down		12	19	mA	CS = V_{IH}, V_{DD} = 12.6V

7245 PIN DESCRIPTION

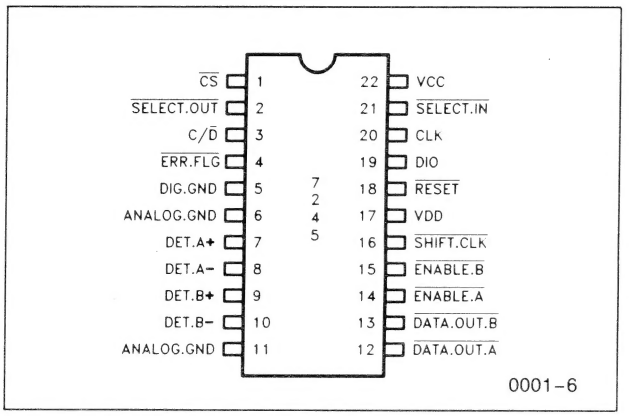


Figure 6. 7245 Pin Configuration

Table 3. 7245 Pin Description

Symbol	Pin No.	I/O	Source/Destination	Description
$\overline{CS}$	1	I	External	An active low signal used for multiplexing of FSAs. The FSA is disabled whenever $\overline{CS}$ is high.
$\overline{SELECT.OUT}$	2	O	7245 FSA	The $\overline{SELECT.IN}$ pulse delayed by two clocks and connected to the $\overline{SELECT.IN}$ pin of the next FSA. It is delayed by two clocks because the FSA is a dual-channel device. Channel A internally passes $\overline{SELECT.IN}$ to Channel B (delayed by one clock).
C/$\overline{D}$	3	I	7225 BMC	Command/$\overline{Data}$ signal. This signal causes the FSA to enter a receive command mode when high and to interpret the serial data line as data when low. Any previously active command is immediately terminated by C/$\overline{D}$.
$\overline{ERR.FLG}$	4	O	7225 BMC	An error flag used to interrupt the Controller to indicate that an error condition exists. It is an open drain, active low signal.
ANALOG.GND	6, 11			Allows user to design higher noise immunity around detector inputs.
DET.A+, DET.A−, DET.B+, DET.B−	7, 8, 9, 10	I	7114 MBM	Differential signal lines from the MBM detector.
$\overline{DATA.OUT.A}$, $\overline{DATA.OUT.B}$	12, 13	O	7234 CPG	Output data from the FIFO to the CPG generate circuitry. Used to write data into the bubble device (active low).
$\overline{ENABLE.A}$, $\overline{ENABLE.B}$	14, 15	O	7234 CPG/7250	TTL-level outputs utilized as chip selects for other interface circuits. They are set and reset by the Command Decoder under instruction of the BMC (active low).
$\overline{SHIFT.CLK}$	16	I	7225 BMC	A Controller-generated clock signal used to clock data out of the Bubble I/O Output Latch to the bubble module during a write operation and to cause bubble signals to be converted by the Sense Amp and clocked into the Bubble I/O Input Latch on a read.

Table 3. 7245 Pin Description (Continued)

Symbol	Pin No.	I/O	Source/Destination	Description
$\overline{\text{RESET}}$	18	I	7225 BMC	An active low signal that resets all flags and pointers in the FSA as well as disabling the chip as the $\overline{\text{CS}}$ signal does. The $\overline{\text{RESET}}$ pulse width must be 5 clock periods to assure the FSA is properly reset.
DIO	19	I/O	7225 BMC	The Serial Bus data line (a bidirectional active high signal).
CLK	20	I	Clock	Same TTL-level clock used to generate internal timing as used for 7225.
$\overline{\text{SELECT.IN}}$	21	I	7225 BMC	An input utilized for time-division multiplexing. An active low signal whose presence indicates that the FSA is to send or receive data from the Serial Bus during the next two clock periods.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... −40°C to +100°C
Storage Temperature ..... −65 to +150°C
Voltage Input ..... −0.5 to 7V
V_{CC} ..... −0.5 to 7V
V_{DD} ..... −0.5 to 14V
Power Dissipation @ 25°C 1W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

D7245 T_A = 0°C to +70°C; V_{CC} = 5.0V +5%, −10%; V_{DD} = 12.0V ±5%
D7245-6 T_A = −40°C to +85°C; V_{CC} = 5.0V +5%, −10%; V_{DD} = 12.0V ±5%

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (All Outputs Except $\overline{\text{SELECT.OUT}}$)			0.45	V	I_{OL} = 3.2 mA
V_{OLSO}	Output Low Voltage ($\overline{\text{SELECT.OUT}}$)			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage (All Outputs Except $\overline{\text{SELECT.OUT}}$)	2.4			V	I_{OH} = 400 µA
V_{OHSO}	Output High Voltage ($\overline{\text{SELECT.OUT}}$)	2.4			V	I_{OH} = 200 µA
$\lvert I_{OFLE} \rvert$	Output Float Leakage ($\overline{\text{ERR.FLAG}}$)			10	µA	$0.45 \le V_{OUT} \le V_{CC}$
$\lvert I_{IN} \rvert$	Input Leakage Current			10	µA	$0 \le V_{IN} \le V_{CC}$
$\lvert I_{OFL} \rvert$	Output Float Leakage (DIO)			100	µA	$0.45 \le V_{OUT} \le V_{CC}$
I_{CC}	Power Supply Current from V_{CC}			120	mA	
I_{DD}	Power Supply Current from V_{DD}			30	mA	

7250 PIN DESCRIPTION

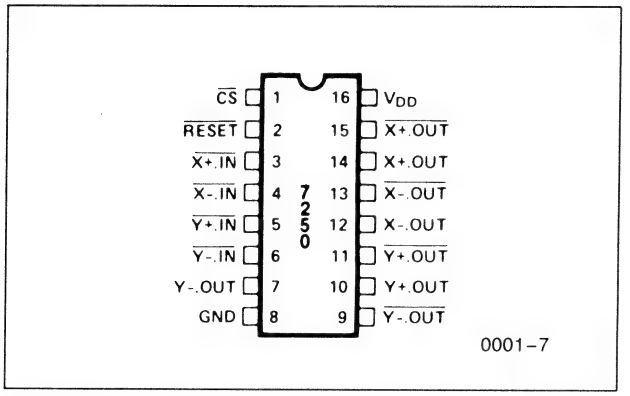


Figure 7. 7250 Pin Configuration

Table 4. 7250 Pin Description

Symbol	Pin No.	I/O	Source/Destination	Description
$\overline{CS}$	1	I	7245 FSA	Chip select. It is active low. When high, chip is deselected and I_{DD} is significantly reduced.
$\overline{RESET}$	2	I	7225 BMC	Active low input from $\overline{RESET.OUT}$ of 7225 Controller forces 7250 outputs inactive so that bubble memory is protected in the event of power supply failure.
$\overline{X+.IN}$, $\overline{X-.IN}$	3, 4	I	7225 BMC	Active low inputs from Controller that turn on the high-current X outputs.
$\overline{Y+.IN}$, $\overline{Y-.IN}$	5, 6	I	7225 BMC	Active low inputs from Controller that turn on the high-current Y outputs.
Y − .OUT $\overline{Y-.OUT}$ Y + .OUT $\overline{Y+.OUT}$	7, 9, 10, 11	O	7254	High-current outputs and their complements for driving gates of the 7254 transistors, which in turn drive the Y coils of the bubble memory.
X − .OUT $\overline{X-.OUT}$ X + . OUT $\overline{X+.OUT}$	12, 13, 14, 15	O	7254	High-current outputs and their complements for driving gates of the 7254 transistors, which in turn drive the X coils of the bubble memory.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65° to +150°C
Voltage Input ..... −0.5 to V_{DD} +0.5V
Output Current ..... 250 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

SI7250 T_A = 0°C to +70°C; V_{DD} = 12.0V +5%, −10%
SI7250-6 T_A = −40°C to +85°C; V_{DD} = 12.0V +5%, −10%

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
$\|I_{IN}\|$	Input Current			5	μA	V_I = 0.8V
V_{IL}	Low-Level Input Voltage			0.8	V	
V_{IH}	High-Level Input Voltage	2.2			V	
I_{DD0}	Supply Current			4.5	mA	Chip Deselected: $\overline{CS}$ = V_{IH}, V_{DD} = 12.6V
I_{DD1}	Supply Current			75	mA	f = 100 kHz, V_{DD} = 12.6V, Output Unloaded

7254 PIN DESCRIPTION

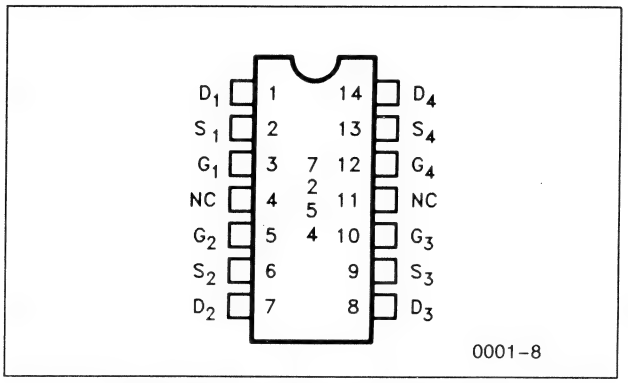


Figure 8. 7254 Pin Configuration

Table 5. 7254 Pin Description

Symbol	Pin No.	I/O	Source/Destination	Description
D_1	1	O	7114 MBM	Coil Drive Current
S_1	2	I	Ground	
G_1	3	I	7250 CPD	Gate Drive Signal
G_2	5	I	7250 CPD	Gate Drive Signal
S_2	6	I	+12V	
D_2	7	O	7114 MBM	Coil Drive Current
D_3	8	O	7114 MBM	Coil Drive Current
S_3	9	I	Ground	
G_3	10	I	7250 CPD	Gate Drive Signal
G_4	12	I	7250 CPD	Gate Drive Signal
S_4	13	I	+12V	
D_4	14	O	7114 MBM	Coil Drive Current

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +150°C
Gate Voltage 15V
Power Dissipation @ 80°C 0.98W
Power Dissipation @ 25°C 1.75W
Continuous Drain Current 2A
Peak Drain Current
(Pulsed; pulse width ≤300 μs;
duty cycle ≤1%) 3A

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

VQ7254 T_A = −40°C to +85°C; all limits apply for N- and P-Channel transistors

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
BV_{DSS}	Drain-Source Breakdown Voltage	20			V	V_{GS} = 0, I_D = 10 μA
$V_{GS}(th)$	Gate-Source Threshold Voltage	0.8			V	V_{GS} = V_{DS}, I_D = 1 mA, T_A = 25°C
		0.65			V	V_{GS} = V_{DS}, I_D = 1 mA, T_A = 85°C
I_{GSS}	Gate Leakage Current			100	nA	V_{GS} = 12V, V_{DS} = 0, T_A = 25°C
I_{DSS}	Drain Leakage Current			500	nA	V_{GS} = 0, V_{DS} = 20V, T_A = 25°C
R_{DS}	On-Resistance for sum of Q1 + Q2, Q3 + Q4 (Note 1)	2.0	2.5	3.0	Ω	V_{GS} = 11.4V, 1_D = 1A, T_A = 25°C
V_{F1}	Parasitic Diode Forward Voltage (Note 1)			0.75	V	V_{GS} = 0V, I_D = 50 mA, T_A = 25°C
V_F2	Parasitic Diode Forward Voltage (Note 1)			1.20	V	V_{GS} = 0V, I_D = 1A, T_A = 25°C

NOTE:
Pulse test—300 μs pulse, 1% duty cycle, r_{DS} increase 0.8%/°C.

TECHNOLOGY CORPORATION
101 BLUE RAVINE ROAD
FOLSOM, CA 95630

MARKETING, CUSTOMER SERVICE: (408) 980-5300
TECHNICAL HOTLINE: (916) 351-3132
FAX: (408) 980-5383
TELEX: 910 250 1368 MEMTECH UQ
EASYLINK: 62020974

MemTech does not assume any responsibility for use of any circuitry described. No circuit patent licenses are implied and MemTech reserves the right to change said circuitry and specifications at any time without notice. MemTech assumes no responsibility for any errors that may appear in the document and makes no commitment to update nor to keep current the information contained in this document.

Printed in U.S.A/1187/5K/RJ/DT

PRODUCT RELEASE NOTE

BPK74 DATA SHEET ERRATA

Page 3 - BPK74 Temperature Range

Non-volatile storage column

Reads: -20°C to +70°C; should be: -20°C to +75°C
Reads: -40°C to +95°C; should be: -40°C to +90°C

Page 4 - 4 Megabit System Schematic

Top center of page - R19-R22 common point returns to + 5 volts (omission)

R17 - Delete

C14 - Change from 15µfd to 0.1µfd +/- 10%

CR3 - Delete and replace with 820KΩ +/- 5%, 1/8W resistor (R23)

Page 5 - Absolute maximum ratings

Change 7114-4 to 7114. Ratings apply to all versions of 7114.

Page 8 - D7234 DC characteristics

General Conditions (top of table)

Reads: 5.0V + 5% (two places)
Should read: 5.0V +/- 5%